REMARKS

Applicants respectfully request consideration of the subject application. Applicants amended claims 1, 7, 12, 15, and 17 to clarify the limitations already present in the claims, thus the amendments are non-narrowing and do not add new matter.

The Office Action refers to reference "Ray et al (US 6, 631, 130)." Applicants based the following remarks on the assumption that the Office Action referred to Roy et al. (US 6,631,130).

Claim Objections

Claim 17 has been objected to because it depends on a non-existing claim 18. The Examiner has examined the application under the assumption that claim 17 depends on claim 15. Claim 17 is amended herewith to claim dependency to claim 15.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 1-6

Claims 1 and 6 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,631,130 to Roy et al. ("Roy"), in view of Hamlin et al. (HAMLIN Jr., R.W., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), ("Hamlin").

Claim 1

Claim 1 requires selecting <u>a subset of path overhead bytes</u> from said plurality of path overhead bytes. Moreover, claim 1 requires determining a signal number and path overhead number <u>for each byte of said subset of path overhead bytes</u>.

Roy describes a network switch that includes at least one port processor and at least one switch element. (Roy, Abstract). The port processor has a SONET OC-x interface, a UTOPIA interface, and an interface to the switch element. (Roy, Abstract). The port processor further includes a serial to parallel converter 12, a SONET framer and transport overhead (TOH) extractor 14, a high order pointer processor 16, and a POH extractor 18. (Roy, col. 5, ll. 22-27). The POH extractor processes <u>all</u> the nine bytes of Path Overhead in each of the forty-eight SONET SPES. (Roy, Figure 1 and col. 10, ll. 54-55).

Hamlin describes a SONET overhead terminator-3 (SOT-3) chip that terminates overhead at network boundaries for STS-3, STS3C, and STM-1 applications. (Hamlin, p. 276). The SOT-3 features include overhead extraction, overhead insertion, alarm signal detection, alarm signal generation, performance monitoring, pointer tracking, pointer generation, payload retiming, and payload realignment. (Hamlin, p. 276). <u>All</u> incoming and outgoing overhead bytes and the performance monitoring are stored in an on-chip static RAM. (Hamlin, p. 277). A special queue manager and a unique RAM controller were designed to prioritize and process access requests between the FIFO's and registers. (Hamlin, p. 277 and Figure 3). <u>All</u> nine bytes of the transport overhead (includes the section overhead and the line overhead bytes) are then stored in FIFO's. (Hamlin, p. 278). The POH

bytes are then stored in the POH register. (Hamlin, p. 278).

Therefore, the combination describes a network switch that includes at least one port processor and at least one switch element according to Roy. The SONET interface of the port processor is implemented using one SOT-3 chip per STS-3 of the network switch to handle overhead extraction, overhead insertion, alarm detection, alarm signal generation, performance monitoring, pointer tracking, pointer generation, payload retiming, and payload realignment according to Hamlin. As according to Hamlin, the SOT-3 stores all the incoming and the outgoing overhead bytes, as well as all the performance monitor counters in an on-chip RAM.

Claim 1 selects a subset of path overhead bytes, determines a signal number and path overhead number for each byte of the subset, and stores this information in a RAM FIFO. Conversely, the combination stores all the overhead bytes of a SONET/SDH signal including all path overhead bytes of the SONET/SDH. Furthermore, the combination does not store both the signal number and the path overhead number for each byte of the subset in a RAM FIFO. Thus, the combination does not allow the flexibility of storing a few or none of the POH bytes of one or more synchronous payload envelopes from a SONET/SDH signal because all overhead bytes are stored.

Because the combination does not describe selecting a subset of path overhead bytes from said plurality of path overhead bytes, and determining a signal number and path overhead number for each byte of said subset of path overhead bytes, the combination fails to render claim 1 obvious.

Claims 2-6

Applicants respectfully submit that claims 2-6 are dependent directly or indirectly on claim 1, thus include the same limitations as claim 1. As such, claims 2-6 are patentable for at least the same reasons as claim 1.

Claims 7-11 and 15-17

Claims 7, 15 and 16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Roy in view of Hamlin, and U.S. Patent No. 5,559,969 to Jennings ("Jennings").

Claim 7

Claim 7 requires selecting <u>one or more bytes of said plurality of path overhead bytes</u>. Moreover, claim 7 requires determining a signal number and a path overhead number <u>for each byte of said path overhead bytes selected</u>.

As discussed above, Roy describes a network switch that includes at least one port processor and at least one switch element. (Roy, Abstract). Hamlin, also discussed above, describes a SONET overhead terminator-3 (SOT-3) chip that terminates overhead at network boundaries for STS-3, STS3C, and STM-1 applications. (Hamlin, p. 276).

Jennings describes a system whereby a number of processors may communicate with a memory element and wherein the memory element may operate at a lower speed without substantially reducing the band pass of a computer system. (Jennings, col. 3, ll. 22-27).

Therefore, the combination describes a computer system of Jennings whereby a number of processors communicate with a memory element connected to a network switch that includes at least one port processor and at least one switch element according to Roy. The SONET interface of the port processor is implemented using one SOT-3 chip per STS-3 of the network switch to handle overhead extraction, overhead insertion, alarm detection, alarm signal generation, performance monitoring, pointer tracking, pointer generation, payload retiming, and payload realignment according to Hamlin. As according to Hamlin, the SOT-3 stores all the incoming and the outgoing overhead bytes, as well as all the performance monitor counters in an on-chip RAM.

Claim 7 selects one or more bytes of said plurality of path overhead bytes, determines a signal number and path overhead number for each byte selected, and stores this information in a RAM FIFO. Conversely, the combination stores all the overhead bytes of a SONET/SDH signal including all path overhead bytes of the SONET/SDH. Furthermore, the combination does not store both the signal number and the path overhead number for each byte selected in a RAM FIFO. Thus, the combination does not allow the flexibility of storing a few or none of the POH bytes of one or more synchronous payload envelopes from a SONET/SDH signal because all overhead bytes are stored.

Because the combination does not describe selecting one or more bytes of said plurality of path overhead bytes and determining a signal number and a path overhead number for each byte of said path overhead bytes selected, the combination fails to render claim 7 obvious.

Claims 8-11

Applicants respectfully submit that claims 8-11 are dependent directly or indirectly on claim 7, thus include the same limitations as claim 7. As such, claims 8-11 are patentable for at least the same reasons as claim 7.

Claim 15

Claim 15 requires a first RAM FIFO buffer having a first plurality of entries for storing a first set of path overhead bytes derived from a group of one or more bytes selected from a plurality of path overhead bytes for a synchronous payload envelope. Moreover, claim 15 requires a second RAM FIFO buffer having a second plurality of entries for storing a second set of path overhead bytes derived from one or more bytes of said plurality of path overhead bytes for said synchronous payload envelope. Claim 15 also requires in each RAM FIFO buffer a first section for storing a path overhead byte, a second section for storing at least a portion of a signal number (S#), and a third section for storing a path overhead number (P#) that correlates to which path overhead byte of said synchronous payload envelope is stored.

As discussed above, the combination describes a computer system of Jennings whereby a number of processors communicate with a memory element connected to a network switch that includes at least one port processor and at least one switch element according to Roy. The SONET interface of the port processor implemented using one SOT-3 chip per STS-3 of the network switch to handle overhead extraction, overhead insertion, alarm detection, alarm signal generation,

performance monitoring, pointer tracking, pointer generation, payload retiming, and payload realignment according to Hamlin. As according to Hamlin, the SOT-3 stores all the incoming and the outgoing overhead bytes, as well as all the performance monitor counters in an on-chip RAM. With all the POH bytes ultimately stored in a POH register.

Claim 15 requires a first and second RAM FIFO for storing sets of path overhead bytes derived from a group of one or more bytes selected from a plurality of path overhead bytes for a synchronous payload envelope, wherein each of the entries comprises a first section for storing a path overhead byte, a second section for storing at least a portion of a signal number (S#), and a third section for storing a path overhead number (P#) that correlates to which path overhead byte of said synchronous payload envelope is stored. Conversely, the combination stores all the overhead bytes of a SONET/SDH signal including all path overhead bytes of the SONET/SDH. Furthermore, the combination does have sections in RAM FIFO for storing both the signal number and the path overhead number that correlates to which path overhead byte of said synchronous payload envelope is stored. Thus, the combination does not allow the flexibility of storing a few or none of the POH bytes of a synchronous payload envelope from a SONET/SDH signal because all overhead bytes are stored.

Because the combination does not describe RAM FIFO buffers having a first plurality of entries for storing a first set of path overhead bytes derived from a group of one or more bytes selected from a plurality of path overhead bytes for a synchronous payload envelope and each RAM FIFO buffer having a first section for

storing a path overhead byte, a second section for storing at least a portion of a signal number (S#), and a third section for storing a path overhead number (P#) <u>that correlates to which path overhead byte of said synchronous payload envelope is stored</u>, the combination fails to render claim 15 obvious.

Claims 16 and 17

Applicants respectfully submit that claims 16 and 17 are dependent directly or indirectly on claim 15, thus include the same limitations as claim 15. As such, claims 16 and 17 are patentable for at least the same reasons as claim 15.

Claims 12-14

Claims 12 and 13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hamlin in view of Roy.

Claim 12

Claim 12 requires a RAM FIFO buffer having a plurality of entries, each entry comprising a first section for storing a path overhead byte <u>selected from a plurality of path overhead bytes</u>, a second section for storing a signal number (S#) and a third section for storing a path overhead number (P#) <u>that correlates to which path overhead byte of said synchronous payload envelope is stored</u>.

As discussed above, the combination of Roy and Hamlin describes a network switch that includes at least one port processor and at least one switch element according to Roy. The SONET interface of the port processor implemented using

one SOT-3 chip per STS-3 of the network switch to handle overhead extraction, overhead insertion, alarm detection, alarm signal generation, performance monitoring, pointer tracking, pointer generation, payload retiming, and payload realignment according to Hamlin. As according to Hamlin, the SOT-3 stores <u>all the incoming and the outgoing overhead bytes</u>, as well as all the performance monitor counters in an on-chip RAM.

Claim 12 requires a RAM FIFO for storing path overhead bytes <u>selected from a plurality of path overhead bytes</u>, <u>a signal number</u>, and <u>a path overhead number that correlates to which path overhead byte of said synchronous payload envelope</u> is stored in separate sections. Conversely, the combination stores <u>all the overhead bytes</u> of a SONET/SDH signal including <u>all path overhead bytes</u> of the SONET/SDH. Furthermore, the combination does have sections in RAM FIFO for storing both the signal number and the path overhead number <u>that correlates to which path overhead byte of said synchronous payload envelope is stored</u>. Thus, the combination does not allow the flexibility of storing a few or none of the POH bytes of a synchronous payload envelope from a SONET/SDH signal because <u>all overhead bytes are stored</u>.

Because the combination does not describe a RAM FIFO buffer having a plurality of entries, each entry comprising a first section for storing a path overhead byte <u>selected from a plurality of path overhead bytes</u> a second section for storing a signal number (S#) and a third section for storing a path overhead number (P#) <u>that correlates to which path overhead byte of said synchronous payload envelope is stored</u>, the combination fails to render claim 12 obvious.

Claims 13 and 14

Applicants respectfully submit that claims 13 and 14 are dependent directly or indirectly on claim 12, thus include the same limitations as claim 12. As such, claims 13 and 14 are patentable for at least the same reasons as claim 12.

Conclusion

If the allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact the undersigned at (408) 720-8300. If there are any additional charges, please charge our Deposit Account No. 02–2666.

Respectfully submitted,

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Dated: 2/9, 2006

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